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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,846	06/27/2003	David B. Glasco	NWISP030	8732

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,846	GLASCO, DAVID B.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed May 17, 2006. This amendment has been entered and carefully considered. Claims 1-35 remain pending in the application.

2. Applicant's arguments with respect to claims 1-35 have been considered but are deemed to be moot in view of the new grounds of rejection. The finality of the previous office action is hereby withdrawn. Any inconvenience is *SINCERELY* regretted.

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edirisooriya et al. (2003/0195939A1);

hereinafter Edi; in view of Iwasa et al. (5,241,641); hereinafter Iwasa.

As per claim 1, Edi discloses a computer system, comprises plurality of processors 12 and 14, cache coherence controllers 26 and 28 (e.g. see figure 1), the first processor 12 and the home cache coherence controller 26 are interconnected (e.g. see figure 1); a remote processor 14 including a remote cache coherence controller 28 (e.g. see figure 1), the remote cache coherence controller configured to receive a probe from the home processor, identify a processor that owns a cache line, and send a targeted probe to the processing processor; for example, Edi discloses that if a CRIL request to the same cache block is found in the request queue 30 (block 202), then the processor 12 determines whether the cache block associated with the CRIL request is in an owned state at block 204, and if the cache block is in an owned state at block 204, then the processor 12 generates a HITM signal on the interconnection network 16 (block 206) (e.g. see page 3, para. [0024], lines 7 et seq.). Edi discloses the invention as claimed; Eli clearly indicated, starting at para. [0018] that while only two processors (i.e., the processors 12 and 14) are shown in the example in FIG. 1, persons of ordinary skill in the art will recognize that ***the multiprocessor system 10 may include additional processors or agents that are also communicatively coupled via the***

interconnection network 16, if desired. Edi with only one exception, does not suggest clusters/nodes of processors including home cluster and remote cluster and wherein the plurality of processing nodes and the cache controller interconnected in a point-to-point architecture. Iwasa discloses the missing elements that're known to be required in the system of Edi in order to arrive at Applicant's current invention wherein Iwasa reference is in the same field of endeavor and discloses multiprocessors being arranged in clusters/groups/nodes of processors (e.g. see figure 1) wherein the processor groups/nodes an the cache controller FC2 interconnected in a point-to-point (one-to-one) architecture (e.g. see figure 3; column 3, lines 66 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to look-into the teaching of Iwasa and to implement the multiple processors of Edi in clusters/nodes processors and allowing the processor nodes/cluster connected in a one-to-one (or point-to-point) with the cache controller as taught by Iwasa. In implementing a system of Edi in a multiple nodes and point-to-point architecture, it would eliminate or reduce the need to have individual nodes of the system permanently connected in order to maintain coherent data states over the plurality of distributed nodes; in addition, it would allow information to be shared by

many nodes to enhance performance and data availability. Furthermore, applications can be sped up by executing across multiple nodes and can be scaled-up by adding more transactions to additional nodes which results to improving system throughput, therefore being advantageous.

As per claim 2, Edi discloses wherein the processing unit has the cache line in the owned or modified state as being equivalent to the MESI or MOESI protocols (e.g. see page 2, para. [0016], lines 15-16);

As per claim 3, wherein information for identifying the processing node that owns the cache line is provided in the probe from the home cluster/processor (e.g. see page 3, para. [0022], lines 16-20; page 4, para. [0032], lines 7 et seq.) ;

As per claims 4 and 5; it's known in the memory storage art that the memory coherency protocol of MSI, MESI or MOESI are implemented using directory-base to maintain cache coherency; Edi discloses the conventional cache coherency protocol MSI, MESI and MOESI being implemented in his system; therefore the directory-base implementation is embedded within Edi's system (e.g. see page 2, para. [0016], lines 15-16; para. [0033], lines 6 et seq.); by this rationale, claims 4 and 5 are rejected;

As per claim 6, Edi discloses remote cache coherence controller is further configured to send a directed probe to the processor that owns the cache line associated with the probe; for example, Edi discloses that the CRIL request/command (or probe as

being claimed) is broadcasted/communicated to all of the agents (processor 12, memory controller 20, etc.) within the multiprocessor system 10 via the interconnection network 16 (e.g. see page 2, para. [0019], lines 11 et seq.);

As per claim 7, Edi discloses that the remote cache coherence controller is associated with a pending buffer (queue 30); e.g. see page 3, page [0023], lines 9 et seq.);

As per claim 8, Edi discloses wherein the remote cache coherence controller is set to receive a single response corresponding to the probe by setting the pending buffer (e.g. see page 3, para. [0023], lines 14-18);

As per claim 9, Edi discloses the probe is a read probe (e.g. see page 2, para. [0016], lines 31 et seq.);

As per claim 10, Edi further discloses that the remote cache coherence controller does not send a directed probe if the cache line is also cached shared in the owning cluster (e.g. see page 3, para. [0026], lines 4 et seq., page 4, para. [0032], lines 11 et seq.);

As per claim 11, Edi discloses a request cluster (processor 14) that generates a probe request (CRIL) triggering the probe from the home cluster (e.g. see page 2, para. [0019], lines 6 et seq.);

As per claim 12, Edi discloses wherein each processing node 12 or 14 comprises a processor, a memory controller, and a cache (e.g. see figure 1);

As per claim 13, wherein each processing node has a portion of the computer system address space (e.g. see para. [0015]; lines 4 et seq.) ;

As per claim 14, Edi discloses the home cache coherence controller forwards the probe before probing home cluster processing nodes; for example, the CRIL request is generated by the processor 14 and is broadcasted to all of the other agents within the processor system 10 before internal cache 24 being probed (e.g. see page 2, para. [0019], lines 8 et seq.);

As per claim 15, the further limitation of the home cache coherence controller forwards the probe after sending probes to home cluster processing nodes as being equivalent to the CRIL request is broadcasted (known by the cache controller 28) to all of the other agents within the processor system (e.g. see para. [0019], lines 8 et seq.);

As per claim 16, Edi discloses a method for providing owning node information comprises receiving a request for ownership of a memory line from a request processor (e.g. see para.[0004], lines 1-4), identifying owning processor information associated with the request for ownership at a home processor is equivalently taught as issuing a CRIL request to gain exclusive control by the owing processor of the particular cache block (e.g. see para.[0017], lines 9 et seq.; para.[[0020], lines 20 et seq.); and maintaining owning node information in a coherence directory associated with the home processor thru the implementation of the

MOESI protocol (e.g. see page 2, para.[0016], lines 10-15). Edi discloses the invention as claimed; Eli clearly indicated, starting at para. [0018] that while only two processors (i.e., the processors 12 and 14) are shown in the example in FIG. 1, persons of ordinary skill in the art will recognize that ***the multiprocessor system 10 may include additional processors or agents that are also communicatively coupled via the interconnection network 16, if desired.*** Edi with only one exception, does not suggest clusters/nodes of processors including home cluster and remote cluster and wherein the plurality of processing nodes and the cache controller interconnected in a point-to-point architecture. Iwasa discloses the missing elements that're known to be required in the system of Edi in order to arrive at Applicant's current invention wherein Iwasa reference is in the same field of endeavor and discloses multiprocessors being arranged in clusters/groups/nodes of processors (e.g. see figure 1) wherein the processor groups/nodes an the cache controller FC2 interconnected in a point-to-point (one-to-one) architecture (e.g. see figure 3; column 3, lines 66 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to look-into the teaching of Iwasa and to implement the multiple processors of Edi in clusters/nodes processors and allowing the processor nodes/cluster connected in

a one-to-one (or point-to-point) with the cache controller as taught by Iwasa. In implementing a system of Edi in a multiple nodes and point-to-point architecture, it would eliminate or reduce the need to have individual nodes of the system permanently connected in order to maintain coherent data states over the plurality of distributed nodes; in addition, it would allow information to be shared by many nodes to enhance performance and data availability. Furthermore, applications can be sped up by executing across multiple nodes and can be scaled-up by adding more transactions to additional nodes which results to improving system throughput, therefore being advantageous.

As per claim 17, Edi discloses the request for ownership of the memory line is a read block modify/invalidate request (CRILs) (e.g. see page 2, para.[0016], lines 21-22, also lines 29-30);

As per claim 18, Edi discloses the request for ownership of the memory line is a change to dirty/modified request (e.g. see para. [0022], lines 14-16);

As per claim 19, wherein the request for ownership of the memory line is a validate block request (e.g. see para.[0027-, lines 10-15];

As per claim 20, Edi discloses maintaining owning cluster information in the coherence directory thru the implementation of MSI, MESI or MOESI coherency-directory-base (e.g. see page 2, para.[0016], lines 10-15);

As per claim 21, Edi discloses receiving a subsequent probe

request from the request cluster as being equivalent to after receiving the "backoff" request to wait for cache modification or cache update to be completed, the processor invalidates its copy and SUBSEQUENTLY issues another CRIL request for that particular cache block (e.g. see pages 3-4, para. [0026], lines 10-18);

As per claims 22 and 23, Edi further discloses determining if the state of a memory line associated with the subsequent probe is in the owned or modified state, and sending a targeted probe to an owning cluster if the state is owned or modified (e.g. see para.[0026], lines 19-31);

As per claim 24, wherein the targeted probe includes owning node information (e.g. see para. [0032], lines 7-10);

As per claim 25, erein the targeted probe allows probing of a single processing node (either single processor 12 or processor 14) (e.g. see page 3, para.[0025], lines 1 et seq.);

As per claim 26, Edi discloses an apparatus for providing owning processor information (e.g. see figure 1), the apparatus comprising means for receiving a request (processor or agent; para. [0004], lines 1 et seq.) for ownership of a memory line from a request processor; means for identifying owning processor information associated with the request for ownership at a home processor is equivalently taught the owing processor of the particular cache block issues a CRIL request to gain exclusive control of said cache block (e.g. see para.[0017], lines 9 et seq.; para.[[0020], lines 20 et seq.); and means for maintaining

owning processor information associated with the home processor is taught by cache controller for maintaining owning node/processor/agents information thru the known implementation of hardware base MSI, MESI or MOESI protocol (e.g. see page 1, para. [0003], lines 7 et seq.). Edi discloses the invention as claimed; Eli clearly indicated, starting at para. [0018] that while only two processors (i.e., the processors 12 and 14) are shown in the example in FIG. 1, persons of ordinary skill in the art will recognize that ***the multiprocessor system 10 may include additional processors or agents that are also communicatively coupled via the interconnection network 16, if desired.*** Edi with only one exception, does not suggest clusters/nodes of processors including home cluster and remote cluster and wherein the plurality of processing nodes and the cache controller interconnected in a point-to-point architecture. Iwasa discloses the missing elements that're known to be required in the system of Edi in order to arrive at Applicant's current invention wherein Iwasa reference is in the same field of endeavor and discloses multiprocessors being arranged in clusters/groups/nodes of processors (e.g. see figure 1) wherein the processor groups/nodes an the cache controller FC2 interconnected in a point-to-point (one-to-one) architecture (e.g. see figure 3; column 3, lines 66 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the

current invention was made to look-into the teaching of Iwasa and to implement the multiple processors of Edi in clusters/nodes processors and allowing the processor nodes/cluster connected in a one-to-one (or point-to-point) with the cache controller as taught by Iwasa. In implementing a system of Edi in a multiple nodes and point-to-point architecture, it would eliminate or reduce the need to have individual nodes of the system permanently connected in order to maintain coherent data states over the plurality of distributed nodes; in addition, it would allow information to be shared by many nodes to enhance performance and data availability. Furthermore, applications can be sped up by executing across multiple nodes and can be scaled-up by adding more transactions to additional nodes which results to improving system throughput, therefore being advantageous.

As per claim 27, Edi discloses means for maintaining owning cluster information as being equivalent to the cache controller in each processor, for example, cache controller 26 in processor 12, or cache controller 28 in processor 14 (e.g. see figure 1, para.[0016], lines 10-15);

As per claim 28, means for receiving a subsequent probe request from the request cluster is equivalently taught as after receiving the "backoff" request to wait for cache modification or cache update to be completed, the requested cluster/processor invalidates its copy and SUBSEQUENTLY issues another CRIL request for that particular cache block (e.g. see pages 3-4, para.

[0026], lines 10-18);

As per claims 29 and 30, means for determining (cache controller of the processor) if the state of a memory line associated with the subsequent probe is in the owned or modified state, and sending a targeted probe to an owning cluster if the state is owned or modified (e.g. see para.[0026], lines 19-31);

As per claim 31, wherein the targeted probe includes owning node information (e.g. see para. [0032], lines 7-10);

As per claim 32, wherein the targeted probe allows probing of a single processing node (either single processor 12 or processor 14) (e.g. see page 3, para.[0025], lines 1 et seq.);

As per claims 33-35, the combination of Edi and Iwasa discloses the invention as claimed, detailed above with respect to 16-25 and 26-32; Edi and Iwasa however do not particularly disclose a computer-readable medium of instructions to be implemented on a client computer as being claimed in claims 33-35. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another

system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Edi and Iwasa's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Edi and Iwasa's program on other systems.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/September 03, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100